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|  | **CaLinx2+** | **ML505/XUPv5** | **DE2-70 (with TRDB-LTM, TRDB-D5M)** | **DE3**  **(with MTDB, THDB-ADA)** |
| ***FPGA*** | Xilinx™ VirtexE XCV2000E | Xilinx™ Virtex5 XC5VLX50T (110) | Altera™ Cyclone II EP2C70 | Altera™ Stratix III EP3SL150 (340) |
| ***LUTs/LEs*** | 43K (4LUTs) | 29K (70K) 6LUTs | 68K LEs (4LUTs) | 57K (135K) (8LUTs) |
| ***RAM*** | 655Kb (Block)  614Kb (Distributed) | 2Mb | 1Mb | 5Mb (16Mb) |
| ***Working Freq.*** | 27Mhz | 500Mhz (Tested and Proven) | 250Mhz (Untested, marketing claim) | 500Mhz (Untested, marketing claim) |
| ***On Board Clocks*** | 1 × 27MHz  1 × 25MHz | 1 × 100Mhz, 1 × 33MHz, 1 × 27Mhz  1 × 200Mhz (differential) | 3 × 50MHz  1 × 28.63Mhz | 2 × 50MHz  1 × 24Mhz |
| ***Memory*** |  |  |  |  |
| ***DRAM*** | 2 × 256MB SDRAM | DDR2 SO-DIMM  (256MB Included) | 2 × 32MB SDRAM | DDR2 SO-DIMM  (2GB Included) |
| ***SRAM*** | None | 1MB | 2MB | None |
| ***Flash*** | None | 32MB | 8MB | None |
| ***Removable (Flash)*** | CompactFlash (SystemACE) | CompactFlash (SystemACE) | SD Card | 2 × SD Card |
| ***User Level I/O*** |  |  |  |  |
| ***Slide Switches*** | None | None | 18 | 4 |
| ***DIP Switches*** | 16 | 8 | None | 8 (Tiny) |
| ***Push Buttons*** | 8 | 5 + Dedicated Reset | 4 | 4 |
| ***Rotary Encoder*** | None | 1 | None | None |
| ***7-Segment Display*** | 8 | None | 8 | 2 |
| ***LEDs*** | 8 × Red | 15 × Green | 18 × Red  9 × Green | 8 × RGB |
| ***LCD*** | 16 × 2 Character Matrix | 16 × 2 Character Matrix | 16 × 2 Character Matrix | None |
| ***LCD Screen*** | None | None | 4.3” LCD Touch Panel  (800×480 Res) | 4.3” LCD Touch Panel  (800×480 Res) |
| ***Camera*** | None | None | 1.3 Megapixel (Up to 15 fps) | None |
| ***Ethernet*** | 4 × 10/100 (PHY Interface) | 1 × 10/100/1000 (PHY Interface) | 1 × 10/100 (MAC Interface) | 1 × 10/100 (PHY Interface) |
| ***High-Speed Network*** | None | SMA, SATA, SFP | None | None |
| ***USB*** | 1 (PHY) | 1 × Host  1 × Device | 1 × Host  1 × Device | 2/3 × Host  1/0 × Device (Chosen by jumper) |
| ***RS232*** | 2 | 1 | 1 | 1 |
| ***PS/2*** | 1 | 2 | 1 | 1 |
| ***ADC / DAC*** | 1 × ADC | None | None | 2 × High-Speed ADC  2 × High-Speed DAC |
| ***Video In*** | 1 × TV In (NTSC) | 1 × VGA In (10-bit) | 2 × TV In (NTSC) | 1 × TV In (NTSC) |
| ***Video Out*** | 1 × TV Out (NTSC)  1 × S-Video Out (NTSC) | 1 × DVI Out | 1 × VGA Out (10 bit) | 1 × VGA Out (10 bit) |
| ***Audio In*** | 1 × Mic  1 × Stereo | 1 × Mic  1 × Line In (Stereo) | 1 × Mic  1 × Line In (Stereo) | 1 × Mic  1 × Line In (Stereo) |
| ***Audio Out*** | 1 × Headphones  1 × Stereo | 1 × Headphones  1 × Line Out (Stereo) | 1 x Line Out (Stereo) | 1 x Line Out (Stereo) |
| ***GPIO*** | 120-pin | 1 × 32 single-ended  1 × 16 high-speed differential pair | 2 × 40-pin  GPIO-0: TRDB-D5M  GPIO-1: TRDB-LTM | 4 × 120-pin high-speed  A: 2 × 40-pin *OR* 1 × 120-pin high-speed  B: DDR2 SO-DIMM  C: MTDB (Touch Screen)  D: THDB-ADA (A2D & D2A Board) |
| ***Other I/O*** | ZigBee, 2 × N64 Controller | PCIe 1×, Buzzer, Xilinx XC95144XL CPLD | IrDA | Temp. Sensor |
| ***Synopsis*** | -Dated I/O; Slower FPGA  -Breaking down; No more being built | -Want more rugged/durable design (Plexiglas enclosure)  -Want Heat sink/Fan for FPGA  -Want more GPIO (i.e. Test Headers, RGB LEDs, DIP switches, 7-seg. Display, and radio (Bluetooth or ZigBee)) | +Tested, proven durable design  -Older, low cost FPGA  -I/O downgrade from CaLinx2+  -Geared toward embedded design  -Other schools released solutions | -Graphic interface for generating top-level code; not custom board friendly  -No upgrade in I/O from the CaLinx2+  -Too new of a board  -Too soon to adopt  -Unsuitable for a student lab |

**Recommendations:**

DE2-70

We do not recommend this board because it has an older, low-cost FPGA, is an I/O downgrade from the CaLinx2+, its geared to embedded systems, and other schools have release full solutions to the firmware of the board.

Overall the Altera™ DE2-70 is a good board, but its only benefit above the CaLinx2+ boards is the fact that it is a commercially available and inexpensive board. Otherwise, it offers, at best, roughly the same features as the CaLinx2+, and at worst a severe downgrade. The lack of PHY level Ethernet in particular is quite jarring. Coupled with the cost of changing the lab, and losing much of the existing course work, the Altera™ DE2-70 is not an upgrade for EECS150 and would be extremely costly in TA and instructor time, independent of any support from Altera™.

For a detailed account, see the DE2-70 Evaluation.

DE3

We do not recommend this board because it’s not much of an upgrade in I/O from the CaLinx2+, too new of a board, too soon to adopt, and unsuitable for a student lab.

The Altera™ DE3 started off as a very promising board, offering some new and interesting possibilities, including its primary advantage over the CaLinx2+: a newer FPGA and commercial support. However, due to its novelty and physical design, it’s way too early to adopt such a board into the educational setting, and we would expect teething troubles to affect the board for quite some time to come. In short, working with it was an incredibly frustrating experience, and we have no reason yet to suspect students would find it otherwise.

For a detailed account, see the DE3 Evaluation.

ML505

Although the Xilinx™ ML505/XUPv5 has its shortcomings (heat sink and Plexiglas), it is well suited the EECS150 curriculum, and provides a superset of the educational opportunities, offered by the CaLinx2+ boards. The board offers a superset of the CaLinx2+ I/O, including newer and more interesting interfaces, and extends it with a rich set of high-speed interfaces, while offering a more modern FPGA to students. The availability of a large number of diverse interfaces is vital for EECS150, and the ML505/XUPv5 provides just that. Strengthened by the availability of experienced users and high-quality support, this platform is an excellent replacement for the CaLinx2+.

For a detailed account, see the ML505/XUPv5 Evaluation.